CURRICULUM VITAE

SURNAME AND NAME	**STERPONE LUCA**

Italian National Scientific Qualifications awarded for Full Professor positions

Academic Recruitment Field (*"Settore Concorsuale"*)
09/H1 – Sistemi di Elaborazione delle informazioni – I Fascia – Full professor position – since 04.04.2017 to 04.04.2023

Academic Position

Qualification/Title	**Associate Professor**
University	**Politecnico di Torino**
Department	**Dipartimento di Automatica e Informatica**
Academic Recruitment Field (if the candidate holds a position in an Italian University, she/he should insert the *"Settore Concorsuale")*	**09/H1**
Academic Discipline (formally named *"Settore Scientifico Disciplinare",* only for candidates who hold a position in an Italian University)	**ING-ING/05**

Working experience

Dates (from 01/08/2011 to 31/10/2014)	
Name and address of the Employer (Public or/and private institution/body)	**Politecnico di Torino**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department; in case of Italian Universities the candidate is also requested to indicate the *"Settore Scientifico Disciplinare"*)	**Assistant Professor – Rircercatore Universitario Confermato – Dipartimento di Automatica e Informatica**
Main activities/responsibilities	**Research activities on techniques for the automatic design**

Dates (from 15/04/2008 to 31/07/2011)	
Name and address of the Employer (Public or/and private institution/body)	**Politecnico di Torino**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department; in case of Italian Universities the candidate is also requested to indicate the *"Settore Scientifico Disciplinare"*)	**Research Assistant – Assegnista di ricerca – Dipartimento di Automatica e Informatica**
Main activities/responsibilities	**Post-Doc Fellowships in the area of "Information Technology"**

Dates (from 01/01/2007 to 14/04/2008)	
Name and address of the Employer (Public or/and private institution/body)	**Politecnico di Torino**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School	**Research Assistant – Assegnista di ricerca –**

and the Department; in case of Italian Universities the candidate is also requested to indicate the *"Settore Scientifico Disciplinare"*)	**Dipartimento di Automatica e Informatica**
Main activities/responsibilities	**Scientific research in the field of the FP6-IST-MAP2 european project entitled "Development of optimization method for the energetic consumption and the dependability of circuits and digital systems"**

Education and Training (please use the following table to describe Degrees awarded, by only indicating the information concerning Bachelor's Degree, Master of Science's Degree or/and PhD)

Date	**27/03/2007**
Institution which issued the degree	**Politecnico di Torino**
Type of Degree awarded (only Bachelor's Degree, Master of Science's Degree, PhD)	**PhD title in System and Computer Engineering – Ingegneria Informatica e dei Sistemi**

Date	**17/11/2003**
Institution which issued the degree	**Politecnico di Torino**
Type of Degree awarded (only Bachelor's Degree, Master of Science's Degree, PhD)	**Master Degree in Computer Engineering**

FUNDAMENTAL RESEARCH OVERVIEW

1. Scientific Activity

The research activity of Luca Sterpone results in the production of **184 publications** in the period 2004.01 – 2020.02. The publications are classified, per year, as follows:

- **2** Springer books
- **3** Book chapters: 1 Springer, 1 Wiley&Sons, 1 IGI
- **54** Journal Manuscripts ACM/IEEE Transactions/Elsevier
- **125** Papers included within international conference proceedings with peer-review of IEEE or ACM conference.

1.1 The three most important outcomes/results of the research activity of Luca Sterpone are:

A1. L. Sterpone, M. Violante, "A new reliability-oriented place and route algorithm for SRAM-based FPGAs", **IEEE Transactions on Computers**, Vol. 55, Issue 6, June, 2006, pp. 732 – 744, DOI: 10.1109/TC.2006.82
ANVUR 09/H1: 1

A2. L. Sterpone, M. Porrmann, J. Hagemeyer, "A Novel Fault Tolerant and Runtime Reconfigurable Platform for Satellite Payload Processing", **IEEE Transactions on Computers**, Vol. 62, Issue 8, June, 2013, pp. 1508 – 1525, DOI: 10.1109/TC.2013.80
ANVUR 09/H1: 1

A3. M. Sonza Reorda, L. Sterpone, A. Ullah, "An Error-Detection and Self-Repairing Method for Dynamically and Partially Reconfigurable Systems", **IEEE Transactions on Computers**, Vol. 66, Issue 6, June, 2017, pp. 1022 – 1033, DOI: 10.1109/TC.2016.2607749
ANVUR 09/H1: 1

1.2 Complete Overview of all the significant publications of the candidate

Ruolo	Year	Conference Proceedings	Journals	Book	Book Chapter	Totale
Professore Associato	**2020**	**2**	**1**			**3**
Professore Associato	**2019**	**9**	**4**			**13**
Professore Associato	**2018**	**10**	**2**			**12**
Professore Associato	**2017**	**9**	**6**			**15**
Professore Associato	**2016**	**7**	**3**			**10**
Professore Associato	**2015**	**3**	**3**			**6**
Ricercatore	**2014**	**9**	**6**			**15**
Ricercatore	**2013**	**8**	**3**			**11**
Ricercatore	**2012**	**10**				**10**
Assegnista/Ricercatore	**2011**	**5**	**2**		**1**	**8**
Assegnista	**2010**	**7**	**4**	**1**	**1**	**13**
Assegnista	**2009**	**7**	**3**			**10**
Assegnista	**2008**	**10**	**6**	**1**	**1**	**18**
Assegnista	**2007**	**14**	**4**			**18**
Dottorando	**2006**	**7**	**4**			**11**
Dottorando	**2005**	**7**	**2**			**9**
Dottorando	**2004**	**1**	**1**			**2**
Totale		**125**	**54**	**2**	**3**	**184**

2. Teaching activity

- Formal responsibility of Bachelor's (Laurea) and Master of Science's (Laurea Magistrale) degree courses in Italian and/or foreign universities.
    - Computer Science, Politecnico di Torino, Italian language, 9 years, (A.A. 2010/2011, 2011/2012, 2012/2013, 2013/2014, 2014/2015, 2015/2016, 2016/2017, 2017/2018, 2018/2019)
    - Operative Systems, Politecnico di Torino, Italian language, 6 years (A.A. 2014/2015, 2015/2016, 2016/2017, 2017/2018, 2018/2019, 2019/2020)
    - Computer Architecture, Politecnico di Torino, Italian language, 2 years (A.A. 2018/2019, 2019/2020)
- Formal responsibility of PhD courses in Italian and/or foreign universities.
    - Reconfigurable Computing, English, 6 years (A.A. 2014/2015, 2015/2016, 2016/2017, 2017/2018, 2018/2019, 2019/2020)
- Formal responsibility of Specializing Master's courses and Life Learning courses in Italian and/or foreign universities in PhD courses.

The following table provides, for each academic year, the number of courses and the teaching role.

Ruolo	Year	PhD Course	Formal Responsible	Assistant	Tutor
Professore Associato - Vice Direttore	2019/2020	1	2		
Professore Associato	2018/2019	1	3		
Professore Associato	2017/2018	1	2	1	
Professore Associato	2016/2017	1	2	1	
Professore Associato	2015/2016	1	2	2	
Professore Associato	2014/2015	1	2	2	
Ricercatore	2013/2014		1	2	
Ricercatore	2012/2013		1	2	1
Ricercatore	2011/2012		1	2	1
Assegnista	2010/2011		1	2	1
Assegnista	2009/2010			2	1
Assegnista	2008/2009			3	1
Assegnista	2007/2008			3	1
Dottorando	2006/2007			1	1
Dottorando	2005/2006			1	1
Dottorando	2004/2005			1	1

3. Institutional offices and roles in Italian and foreign Universities and/or public and private institutions with scientific and/or technology transfer aims

- Luca Sterpone is **Vice Head** of the Dipartimento di Automatica e Informatica (DAUIN), Politecnico di Torino, since 09/10/2019
- Luca Sterpone is member of the election commission of the Computer and System Engineering Department (DAUIN)
- Luca Sterpone è stato nominato componente della commissione giudicatrice di una valutazione per professore universitario di ruolo di II fascia, Settore Concorsuale 09/H1, Settore Scientifico Disiplinare ING-ING/05 presso il Dipartimento di Automatica e Informatica, con Decreto Rettorale n. 549 del 3 giugno 2019.
- Luca Sterpone is the responsible of the Advisory Board of the "Collegio di Ingegneria Informatica, del Cinema e Meccatronica" (Faculty of Computer, Multimedia and Mechatronic Engineering)
- Luca Sterpone is the responsible of Relation with Companies in the framework of the commission of "Tirocini e Rapporti con le Imprese" (Training and Relation with Companies)

Scientific publications Luca Sterpone

The research activity of Luca Sterpone results in the production of 184 publications in the period 2004.01 – 2020.02. The publications are classified, per year, as follows:

Ruolo	Year	Conference Proceedings	Journals	Book	Book Chapter	Totale
Professore Associato	**2020**	**2**	**1**			**3**
Professore Associato	**2019**	**9**	**4**			**13**
Professore Associato	**2018**	**10**	**2**			**12**
Professore Associato	**2017**	**9**	**6**			**15**
Professore Associato	**2016**	**7**	**3**			**10**
Professore Associato	**2015**	**3**	**3**			**6**
Ricercatore	**2014**	**9**	**6**			**15**
Ricercatore	**2013**	**8**	**3**			**11**
Ricercatore	**2012**	**10**				**10**
Assegnista/Ricercatore	**2011**	**5**	**2**		**1**	**8**
Assegnista	**2010**	**7**	**4**	**1**	**1**	**13**
Assegnista	**2009**	**7**	**3**			**10**
Assegnista	**2008**	**10**	**6**	**1**	**1**	**18**
Assegnista	**2007**	**14**	**4**			**18**
Dottorando	**2006**	**7**	**4**			**11**
Dottorando	**2005**	**7**	**2**			**9**
Dottorando	**2004**	**1**	**1**			**2**
Totale		**125**	**54**	**2**	**3**	**184**

Book (2)

[L2] N. Battezzati, L. Sterpone, M. Violante, **"Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications"**, Springer,1st Edition, 2010, 220 pp., ISBN: 978-1-4419-7594-2. DOI: 10.1007/978-1-4419-7595-9

[L1] L. Sterpone, "**Electronic System Design Techniques for Safety Critical Applications"**, 2008, Springer, Vol. 26, London (UK), ISBN 978-1-4020-8978-7.
Classificato ISI-like dal 14-01-2009. Presente nelle biblioteche delle seguenti università: ETH Zurich, Stanford, TU Berlin, TU Delft.

Book chapter (3)

[CL3] M. Sonza Reorda, L. Sterpone, M. Violante, **"Advanced technologies for transient faults detection and compensation"**, accepted for publication on IGI Global book, "Design and Test Technology for Dependable Embedded Systems", 2010.

[CL2] Sterpone, L., Collino, F., Camussi, G., Loconsole, C., "**Analysis and clustering of MicroRNA array: A new efficient and reliable computational method**", 2011, Advances in Experimental Medicine and Biology, 696, pp. 679-688., ISBN: 978-1-4419-7045-9. DOI: 10.1007/978-1-4419-7046-6_69

[CL1] L. Sterpone, **"FPGA PAL Design Tools"**, Wiley Encyclopedia of Computer Science and Engineering, 2008, pp. 1316 – 1326, ISBN: 9780470050132

International Journals (54):

[J54] Bozzoli L., Sterpone, L..**An Optimized Frame-Driven Routing Algorithm for Reconfigurable SRAM-based FPGAs**. Acceted for IEEE ACCESS

[J53] Corrado De Sio, C., Azimi, S., Bozzoli, L., Du, B., Sterpone, L.. **Radiation-induced Single Event Transient effects during the reconfiguration process of SRAM-based FPGAs**. MICROELECTRONICS RELIABILITY, ISSN: 0026-2714, doi: 10.1016/j.microrel.2019.06.034

[J52] Corrado De Sio, Sarah Azimi, Luca Sterpone, Boyang Du. **Analyzing Radiation-induced Transient Errors on SRAM-based FPGAs by Propagation of Broadening Effect**. IEEE ACCESS, vol. 7, p. 140182-140189, ISSN: 2169-3536, doi: 10.1109/ACCESS.2019.2915136

[J51] B. Du, L. Sterpone, S. Azimi, D.M. Codinachs, V. Ferlet-Cavrois, C. Polo Boatella, R. Garcia Alia, M. Kastriotou, "**Ultra High Energy Heavy Ion Test Beam on Xilinx Kintex-7 SRAM-based FPGA**", IEEE Transactions on Nuclear Science, 2019, Vol 66, Issue 7, pp. 1813 - 1819

[J50] Sarah Azimi, Boyang Du, Luca Sterpone, David Merodio Codinachs, Raoul Grimoldi, Luca Cattaneo, **A new CAD tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs**. INTEGRATION, vol. 67, p. 73-81, ISSN: 0167-9260, doi: 10.1016/j.vlsi.2019.02.001

[J49] S. Azimi, L. Sterpone, B. Du, L. Boragno, "**On the analysis of radiation-induced Single Event Transients on SRAM-based FPGAs**", Microelectronic Reliability, 2018, Vol. 88-90, pp. 936 – 940. Doi: 10.1016/j.microrel.2018.07.135

[J48] D. Cozzi, S. Korf, L. Cassano, J. Hagemeyer, A. Domenici, C. Bernardeschi, M. Porrmann, L. Sterpone, "**OLTRE²: an On-Line on-demand Testing approach for permanent Radiation Effects in Reconfigurable systems**", vol. 6, no. 4, pp. 511-523, 1 Oct.-Dec. 2018. doi: 10.1109/TETC.2016.2586195

[J47] L. A. Cardona, A. Ullah, L. Sterpone, C. Ferrer, **An FPGA-based dynamically reconfigurable platform for emulation of permanent faults in ASICs.** MICROELECTRONICS RELIABILITY, vol. 75, p. 110-120, ISSN: 0026-2714, doi: 10.1016/j.microrel.2017.06.032

[J46] L. A. Cardona, A. Ullah, L. Sterpone, C. Ferrer, "**A novel tool-flow for zero-overhead cross-domain error resilient partially reconfigurable X-TMR for SRAM-based FPGAs**", November 2017, Elsevier Journal of Systems Architectures, Vol. 81, pp. 112 - 120

[J45] S. Azimi, B. Du, L. Sterpone, "**Evaluation of transient errors in GPGPUs for safety critical applications: an effective simulation-based fault injection environment**", April 2017, Elsevier Journal of Systems Architectures, Vol. 75, pp. 95 - 106

[J44] L. Sterpone, L. Boragno, "**A probe-based SEU detection method for SRAM-based FPGAs**", 2017, Microelectronic Reliability, Vol. 76-77, pp. 154 - 158

[J43] Q. Zhang, S. Azimi, G. La Vaccara, L. Sterpone, B. Du, "**A new approach for Total Ionizing Dose effect analysis on Flash-based FPGAs**", September 2017, Microelectronic Reliability, Vol. 76-77, pp. 58 - 63

[J42] M. Sonza Reorda, L. Sterponem A. Ullah, "**An Error-Detection and Self-Repairing Method for Dynamically and Partially Reconfigurable Systems**", 2017, IEEE Transactions on Computers, Vol. 66, Issue 6, pp. 1022 - 1033

[J41] B. Du, M. Sonza Reorda, L. Sterpone, P. Luis, M. Portela-Garcia, L. Almudena, L. Entrena, "**On-line Test of Control Flow Errors: A new Debug Interface-based approach**", 2016, IEEE Transactions on Computers, Vol. 65, Issue 6, pp. 1846 - 1855

[J40] S. Azimi, B. Du, L. Sterpone, "**On the prediction of Radiation-induced SETs in Flash-based FPGAs**", September 2016, Microelectronic Reliability, Vol. 64, pp. 230 - 234.

[J39] C. Bernardeschi, L. Cassano, A. Domenici, L. Sterpone, "**UA²TPG: An untestability analyser and test pattern generator for SEUs in the configuration memory of SRAM-based FPGAs**", September 2016, Elsevier Integration, Vol. 55, pp. 85 - 97.

[J38] R. Giordano, A. Aloisio, V. Bocci, M. Capodiferro, V. Izzo, L. Sterpone, M. Violante, "**Layout and Radiation Tolerance Issues of High-Speed Links**", 2015, Vol. 62, Issue 6, IEEE Transactions on Nuclear Science, pp. 3177 - 3185.

[J37] L. Sterpone, B. Du, S. Azimi., "**Radiation-induced Single Even Transients modeling and testing on nanometric Flash-based technologies**", 2015, Microelectronics Reliability, Vol. 55, n. 9-10, pp. 2087 – 2091.

[J36] Robinson, W.H. ; Rech, P. ; Aguirre, M. ; Barnard, A. ; Desogus, M. ; Entrena, L. ; Garcia-Valderas, M. ; Guertin, S.M. ; Kaeli, D. ; Kastensmidt, F.L. ; Kiddie, B.T. ; Sanchez-Clemente, A. ; Reorda, M.S. ; Sterpone, L. ; Wirthlin, M., "**Using Benchmarks for Radiation Testing of Microprocessors and FPGAs**", 2015, IEEE Transactions on Nuclear Science, Vol. 62, n. 6, pp. 2547 – 2554.

[J35] L. Parra, A. Lindoso, M. Portela-Garcia, L. Entrena, B. Du, M. Sonza Reorda, L. Sterpone, "**A New Hybrid Nonintrusive Error-Detection Technique Using Dual Control-Flow Monitoring**", 2014, IEEE Transactions on Nuclear Science, Vol. 61, n. 6, pp. 3236 – 3243.

[J34] A. Ullah, L. Sterpone, "**Recovery Time and Fault Tolerance Improvement for Circuits mapped on SRAM-based FPGAs**", 2014, Journal of Electronic Testing, Vol. 30, p. 425 – 442.

[J33] C. Bernardeschi, L. Cassano, A. Domenici, L. Sterpone "**ASSESS: A Simulator of Soft Errors in the Configuration Memory of SRAM-based FPGAs**", 2014, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 33, n. 9, pp. 1342 – 1355.

[J32] D. Sabena, M. Sonza Reorda, L. Sterpone, P. Rech, L. Carro, "**Evaluating the radiation sensitivity of GPGPU caches: new algorithms and experimental results**", 2014, Microelectronics Reliability, Vol. 51, n. 11, pp. 2621 - 2628

[J31] D. Sabena, M. S. Reorda, L. Sterpone, "**On the automatic generation of optimized software-based self-test programs for VLIW processors"**, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22 (4), art. no. 6497676, pp. 813-823.
DOI: 10.1109/TVLSI.2013.2252636

[J30] D. Sabena, L. Sterpone, L. Carro, P. Rech, "**Reliability Evaluation of Embedded GPGPUs for Safety Critical Applications"**, IEEE Transactions on Nuclear Science, 2014, 61, Issue 6, pp. 3123-3129.

[J29] Aloisio, A., Bocci, V., Giordano, R., Izzo, V., Sterpone, L., Violante, M. "**Power consumption versus configuration SEUs in Xilinx Virtex-5 FPGAs**", IEEE Transactions on Nuclear Science, 2013, Vol. 60 (5), pp. 3502-3507.
DOI: 10.1109/TNS.2013.2273001

[J28] Sterpone, L., "**SEL-UP: A CAD tool for the sensitivity analysis of radiation-induced Single Event Latch-Up**", 2013, Microelectronics Reliability, 53 (9-11), pp. 1311-1314.
DOI: 10.1016/j.microrel.2013.07.104

[J27] Sterpone, L., Porrmann, M., Hagemeyer, J. "**A novel fault tolerant and runtime reconfigurable platform for satellite payload processing**", 2013, IEEE Transactions on Computers, 62 (8), pp. 1508-1525.
DOI: 10.1109/TC.2013.80

[J26] Sterpone, L., Battezzati, N., Kastensmidt, F.L., Chipana, R. "**An analytical model of the propagation induced pulse broadening (PIPB) effects on single event transient in flash-based FPGAs**", 2011, IEEE Transactions on Nuclear Science, 58 (5 PART 2), art. no. 5991970, pp. 2333-2340. DOI: 10.1109/TNS.2011.2161886

[J25] L. Sterpone, M. Violante, A. Panariti, A. Bocquillon, F. Miller, N. Buard, A. Manuzzato, S. Gerardin, A. Paccagnella, **"Layout-aware Multi-Cell Upsets Effects Analysis on TMR circuits implemented on SRAM-based FPGAs"**, IEEE Transactions on Nuclear Science, Vol. 58, pp. 2325 – 2332, 2011
DOI: 10.1109/TNS.2011.2161887

[J24] H. Guzman-Miranda, L. Sterpone, M. Violante, M. Aguirre, M. Gutierrez-Rizo, **"Coping With the Obsolescence of Safety- or Mission-Critical Embedded Systems Using FPGAs"**, IEEE Transactions on Industrial Electronics, Issue 99, 2010, 6 pp, DOI: 10.1109/TIE.2010.2050291

[J23] F. Collino, M. Deregibus, S. Bruno, L. Sterpone, G. Aghemo, L. Viltono, C. Tetta, G. Camussi, **"Microvescicles Derived from Adult Human Bone Marrow and Tissue Specific Mesenchymal Stem Cells Shuttle Selected Patterns of miRNAs"**, PlosONE International Medical Journal, 2010, 18 pp., DOI: 10.1371/journal.pone.0011803

[J22] L. Sterpone, V. Ferlet-Cavrois, N. Battezzati, **"Analysis of SET Propagation in Flash-based FPGAs by means of Electrical Pulse Injection"**, IEEE Transactions on Nuclear Science, Vol. 57, Issue 4, August 2010, pp. 1820 – 1826, DOI: 10.1109/TNS.2010.2043686.

[J21] L. Sterpone, **"A new Timing Driven Placement Algorithm for Dependable Circuits on SRAM-based FPGAs"**, 2010, ACM Transactions on Reconfigurable Technology and Systems, 4 (1), art. no. 7, DOI: 10.1145/1857927.1857934

[J20] F. Abate, C. A. Lisboa, L. Carro, L. Sterpone, M. Violante, **"New techniques for improving the performance of the lockstep architecture for SEEs mitigation in FPGA embedded processors"**, IEEE Transactions on Nuclear Science, Volume 56, Issue 4, Part 2, August, 2009, pp. 1992 - 2000. DOI: 10.1109/TNS.2009.2013237

[J19] L. Sterpone, **"A Novel Dual Core Architecture for the Analysis of DNA Microarray Images"**, IEEE Transactions on Instrumentation and Measurement, Volume 58, Issue 8, August 2009, pp. 2653 – 2662, DOI: 10.1109/TIM.2009.2015695.

[J18] N. Battezzati, S. Gerardin, A. Manuzzato, D. Merodio, A. Paccagnella, C. Poivey, L. Sterpone, M. Violante, **"Methodologies to study frequency-dependent Single Event Effects sensitivity in Flash-based FPGAs"**, IEEE Transactions on Nuclear Science, December, 2009, Vol. 56, pp. 3534 – 3541, DOI: 10.1109/TNS.2009.2034316

[J17] N. Battezzati, L. Sterpone, M. Violante, **"Monte Carlo Analysis of the Effects of Soft Error Accumulation in SRAM-based FPGAs"**, IEEE Transactions on Nuclear Science, Volume 55, Issue 6, Part 1, December, 2008, pp. 3381 – 3387, DOI: 10.1109/TNS.2008.2006839

[J16] M. Alderighi, F. Casini, S. D'Angelo, M. Mancini, S. Pastore, L. Sterpone, M. Violante, **"Soft Errors in SRAM-based FPGAs: a comparison of two complementary approaches"**, IEEE Transactions on Nuclear Science, Volume 55, Issue 4, Part 1, August, 2008, pp. 2267 – 2273, DOI: 10.1109/TNS.2008.2000479

[J15] L. Sterpone, M. Violante, **"A new Algorithm for the analysis of the MCUs sensitiveness of TMR architectures in SRAM-based FPGAs"**, IEEE Transactions on Nuclear Science, Volume 55, Issue 4, Part 1, August, 2008, pp. 2019 – 2027, DOI: 10.1109/TNS.2008.2001858

[J14] A. Manuzzato, S. Gerardin, A. Paccagnella, L. Sterpone, M. Violante, **"Effectiveness of TMR-based techniques to mitigate alpha-induced SEU accumulation in commercial SRAM-based FPGAs"**, IEEE Transactions on Nuclear Science, Vol. 55, Issue 4, Part 1, August, 2008, pp. 1968 – 1973, DOI: 10.1109/TNS.2008.2000850

[J13] F. Abate, L. Sterpone, M. Violante, "**A New Mitigation Approach For Soft Errors In Embedded Processors**", IEEE Transactions on Nuclear Science, Vol. 55, Issue 4, Part 1, August, 2008, pp. 2063 – 2069, DOI: 10.1109/TNS.2008.2000839

[J12] C. Bolchini, A. Miele, M. Rebaudengo, F. Salice, D. Sciuto, L. Sterpone, M. Violante, "**Software and Hardware Techniques for SEU Detection in IP Processors**", JETTA: Journal of Electronic Testing: Theory and Applications, Kluwer Academy Publisher, Springer, 2008, pp. 35 – 44, DOI: 10.1007/s10836-007-5028.0

[J11] L. Sterpone, M. Violante, R. Harboe Sorensen, D. Merodio, F. Sturesson, R. Weigand, S. Mattsson, "**Experimental Validation of a Tool for Predicting the Effects of Soft Errors in SRAM-based FPGAs**", IEEE Transactions on Nuclear Science, Vol. 54, No. 6, Part 1, December 2007, pp. 2576-2583, DOI: 10.1109/TNS.2007.910122

[J10] L. Sterpone, M. Violante, "**A New Partial Reconfiguration-based Fault-Injection System to Evaluate SEU Effects in SRAM-based FPGAs",** IEEE Transactions on Nuclear Science, Vol. 54, Issue 4, Part 2, August 2007, pp. 965 – 970, DOI: 10.1109/TNS.2007.904080

[J9] M. Violante, L. Sterpone, A. Manuzzato, S. Gerardin, P. Rech, M. Bagatin, A. Paccagnella, C. Andreani, G. Gorini, A. Pietropaolo, G. Cardarilli, S. Pontarelli, C. Frost, "**A new hardware/software platform and a new 1/E neutron source for soft error studies : testing FPGA at the ISIS facility",** IEEE Transactions on Nuclear Science, Vol. 54, Issue 4, Part 2, August 2007, pp. 1184 – 1189, DOI: 10.1109/TNS.2007.902349

[J8] M. Sonza Reorda, L. Sterpone, M. Violante, F. Lima Kastensmidt, L. Carro, "**Evaluating different solutions to design fault tolerant systems with SRAM-based FPGAs**", JETTA: Journal of Electronic Testing: Theory and Applications, Kluwer Academy Publisher, Vol. 23, No. 1, February, 2007, pp. 47 – 54, DOI: 10.1007/s10836-006-0403-9

[J7] P. Bernardi, L. Sterpone, M. Violante, M- Portela-Garcia "**Hybrid Fault Detection Technique: A Case Study on Virtex-II Pro's PowerPC 405",** IEEE Transactions on Nuclear Science, Vol. 54, Issue 6, December 2006, pp. 3550 – 3557, DOI: 10.1109/TNS.2006.886221

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